

WHAT IS CLAIMED IS:

- 1 1. A transistor having a gate located over a channel region recessed into a semiconductor  
2 substrate, comprising:  
3 a source/drain including a lightly doped region located adjacent said channel region and a  
4 heavily doped region located adjacent said lightly doped region;  
5 an oppositely doped well located under and within said channel region; and  
6 a doped region, located between said heavily doped region and said oppositely doped  
7 well, having a doping concentration profile less than a doping concentration profile of said  
8 heavily doped region.
- 1 2. The transistor as recited in Claim 1 further comprising an oppositely doped buried layer  
2 located under said doped region.
- 1 3. The transistor as recited in Claim 1 wherein said doped region is formed from an  
2 epitaxial layer located over said semiconductor substrate.
- 1 4. The transistor as recited in Claim 1 wherein said source/drain includes P-type lightly and  
2 heavily doped regions and said oppositely doped well is a N-type well, said doped region being a  
3 P-type doped region having a doping concentration profile less than a doping concentration  
4 profile of said P-type heavily doped region.

- 1    5.     The transistor as recited in Claim 1, further comprising:  
2           another source/drain including a lightly doped region located adjacent said channel  
3 region and a heavily doped region located adjacent said lightly doped region; and  
4           another doped region, located between said heavily doped region of said another  
5 source/drain and said oppositely doped well, having a doping concentration profile less than a  
6 doping concentration profile of said heavily doped region of said another source/drain.
- 1    6.     The transistor as recited in Claim 1 further comprising a gate dielectric layer underlying  
2 said gate and gate sidewall spacers about said gate, said transistor further comprising metal  
3 contacts formed over a salicide layer on said gate and said source/drain.
- 1    7.     The transistor as recited in Claim 1 wherein said transistor is a laterally diffused metal  
2 oxide semiconductor device.

1 8. A method of forming a transistor, comprising:  
2 providing a semiconductor substrate;  
3 forming a gate on said semiconductor substrate;  
4 forming a source/drain by:  
5 forming a lightly doped region adjacent a channel region recessed into said  
6 semiconductor substrate, and  
7 forming a heavily doped region adjacent said lightly doped region;  
8 forming an oppositely doped well under and within said channel region; and  
9 forming a doped region between said heavily doped region and said oppositely  
10 doped well, said doped region having a doping concentration profile less than a doping  
11 concentration profile of said heavily doped region.

1 9. The method as recited in Claim 8 further comprising forming an oppositely doped buried  
2 layer recessed into said substrate.

1 10. The method as recited in Claim 8 further comprising forming an epitaxial layer over said  
2 semiconductor substrate, said doped region being formed from said epitaxial layer.

1 11. The method as recited in Claim 1 wherein said source/drain includes P-type lightly and  
2 heavily doped regions and said oppositely doped well is a N-type well, said doped region being a  
3 P-type doped region having a doping concentration profile less than a doping concentration  
4 profile of said P-type heavily doped region.

1    12.    The method as recited in Claim 8, further comprising:  
2            forming another source/drain by:  
3                 forming a lightly doped region located adjacent said channel region, and  
4                 forming a heavily doped region located adjacent said lightly doped region; and  
5            forming another doped region between said heavily doped region of said another  
6    source/drain and said oppositely doped well, said another doped region having a doping  
7    concentration profile less than a doping concentration profile of said heavily doped region of said  
8    another source/drain.

1    13.    The method as recited in Claim 8, further comprising:  
2            forming a gate dielectric layer over said semiconductor substrate;  
3            forming gate sidewall spacers about said gate;  
4            forming a salicide layer on said gate and said source/drain; and  
5            forming metal contacts over said salicide layer on said gate and said source/drain.

1    14.    The method as recited in Claim 8 wherein said transistor is a laterally diffused metal  
2    oxide semiconductor device.

1 15. A semiconductor device on a semiconductor substrate, comprising:  
2 a complementary metal oxide semiconductor device formed on said semiconductor  
3 substrate; and  
4 a laterally diffused metal oxide semiconductor device, including:  
5 a gate located over a channel region recessed into said semiconductor substrate,  
6 a source/drain including a lightly doped region located adjacent said channel  
7 region and a heavily doped region located adjacent said lightly doped region,  
8 an oppositely doped well located under and within said channel region, and  
9 a doped region, located between said heavily doped region and said oppositely  
10 doped well, having a doping concentration profile less than a doping concentration profile of said  
11 heavily doped region.

1 16. The semiconductor device as recited in Claim 15 wherein said complementary metal  
2 oxide semiconductor device includes a source/drain having a heavily doped region with a doping  
3 concentration profile different from said doping concentration profile of said heavily doped  
4 region of said source/drain of said laterally diffused metal oxide semiconductor device.

1 17. The semiconductor device as recited in Claim 15 further comprising another  
2 complementary metal oxide semiconductor device and another laterally diffused metal oxide  
3 semiconductor device on said semiconductor substrate.

1 18. The semiconductor device as recited in Claim 17 wherein said another complementary  
2 metal oxide semiconductor device includes a source/drain having a heavily doped region with a  
3 doping concentration profile different from a doping concentration profile of a heavily doped  
4 region of a source/drain of said another laterally diffused metal oxide semiconductor device.

1 19. The semiconductor device as recited in Claim 17 wherein said complementary metal  
2 oxide semiconductor device is a P-type metal oxide semiconductor device and said another  
3 complementary metal oxide semiconductor device is a N-type metal oxide semiconductor device,  
4 said laterally diffused metal oxide semiconductor device being a P-type laterally diffused metal  
5 oxide semiconductor device and said another laterally diffused metal oxide semiconductor  
6 device being a N-type laterally diffused metal oxide semiconductor device.

1 20. The semiconductor device as recited in Claim 15 wherein said laterally diffused metal  
2 oxide semiconductor device includes an oppositely doped buried layer located under said doped  
3 region.

1 21. The semiconductor device as recited in Claim 15 further comprising an epitaxial layer  
2 located over said semiconductor substrate, said doped region being formed from said epitaxial  
3 layer.

1 22. The semiconductor device as recited in Claim 15 wherein said source/drain includes P-  
2 type lightly and heavily doped regions and said oppositely doped well is a N-type well, said  
3 doped region being a P-type doped region having a doping concentration profile less than a  
4 doping concentration profile of said P-type heavily doped region.

1 23. The semiconductor device as recited in Claim 15 wherein said laterally diffused metal  
2 oxide semiconductor device, further includes:

3 another source/drain including a lightly doped region located adjacent said channel  
4 region and a heavily doped region located adjacent said lightly doped region, and  
5 another doped region, located between said heavily doped region of said another

6 source/drain and said oppositely doped well, having a doping concentration profile less than a  
7 doping concentration profile of said heavily doped region of said another source/drain.

1 24. The semiconductor device as recited in Claim 15 wherein said laterally diffused metal  
2 oxide semiconductor device further includes a gate dielectric layer underlying said gate and gate  
3 sidewall spacers about said gate, said laterally diffused metal oxide semiconductor device further  
4 including metal contacts formed over a salicide layer on said gate and said source/drain.

1 25. The semiconductor device as recited in Claim 15 wherein said complementary metal  
2 oxide semiconductor device includes a gate with a gate dielectric layer underlying said gate and  
3 gate sidewall spacers about said gate, said complementary metal oxide semiconductor device  
4 further including metal contacts formed over a salicide layer on said gate and a source/drain  
5 thereof.

1 26. A method of forming a semiconductor device, comprising:  
2 providing a semiconductor substrate;  
3 forming a complementary metal oxide semiconductor device on said semiconductor  
4 substrate; and  
5 forming a laterally diffused metal oxide semiconductor device, including:  
6 forming a gate on said semiconductor substrate,  
7 forming a source/drain by:  
8 forming a lightly doped region adjacent a channel region recessed into  
9 said semiconductor substrate, and  
10 forming a heavily doped region adjacent said lightly doped region;  
11 forming an oppositely doped well under and within said channel region; and  
12 forming a doped region between said heavily doped region and said oppositely  
13 doped well, said doped region having a doping concentration profile less than a doping  
14 concentration profile of said heavily doped region.

1 27. The method as recited in Claim 26 wherein forming said complementary metal oxide  
2 semiconductor device includes forming a source/drain having a heavily doped region with a  
3 doping concentration profile different from said doping concentration profile of said heavily  
4 doped region of said source/drain of said laterally diffused metal oxide semiconductor device.

1 28. The method as recited in Claim 26 further comprising forming another complementary  
2 metal oxide semiconductor device and forming another laterally diffused metal oxide  
3 semiconductor device on said semiconductor substrate.



1 29. The method as recited in Claim 28 wherein forming said another complementary metal  
2 oxide semiconductor device includes forming a source/drain having a heavily doped region and  
3 forming said another laterally diffused metal oxide semiconductor device includes forming a  
4 source/drain having a heavily doped region, a doping concentration profile of said heavily doped  
5 region of said source/drain of said another complementary metal oxide semiconductor device  
6 being different from a doping concentration profile of said heavily doped region of said  
7 source/drain of said another laterally diffused metal oxide semiconductor device.

1 30. The method as recited in Claim 28 wherein said complementary metal oxide  
2 semiconductor device is a P-type metal oxide semiconductor device and said another  
3 complementary metal oxide semiconductor device is a N-type metal oxide semiconductor device,  
4 said laterally diffused metal oxide semiconductor device being a P-type laterally diffused metal  
5 oxide semiconductor device and said another laterally diffused metal oxide semiconductor  
6 device being a N-type laterally diffused metal oxide semiconductor device.

1 31. The method as recited in Claim 26 wherein forming said laterally diffused metal oxide  
2 semiconductor device includes forming an oppositely doped buried layer recessed into said  
3 semiconductor substrate 32. The method as recited in Claim 26 further comprising forming an  
4 epitaxial layer located over said semiconductor substrate, said doped region being formed from  
5 said epitaxial layer.

1 33. The method as recited in Claim 26 wherein said source/drain includes P-type lightly and  
2 heavily doped regions and said oppositely doped well is a N-type well, said doped region being a  
3 P-type doped region having a doping concentration profile less than a doping concentration  
4 profile of said P-type heavily doped region.

1 34. The method as recited in Claim 26 wherein forming said laterally diffused metal oxide  
2 semiconductor device, further includes:

3 forming another source/drain by:

4 forming a lightly doped region located adjacent said channel region, and

5 forming a heavily doped region located adjacent said lightly doped region, and

6 forming another doped region between said heavily doped region of said another  
7 source/drain and said oppositely doped well, said another doped region having a doping  
8 concentration profile less than a doping concentration profile of said heavily doped region of said  
9 another source/drain.

1 35. The method as recited in Claim 26 wherein forming said laterally diffused metal oxide  
2 semiconductor device, further includes:

3 forming a gate dielectric layer over said semiconductor substrate,

4 forming gate sidewall spacers about said gate,

5 forming a salicide layer on said gate and said source/drain, and

6 forming metal contacts over said salicide layer on said gate and said source/drain.

1 36. The method as recited in Claim 26 wherein forming said complementary metal oxide  
2 semiconductor device, includes:

3 forming a gate dielectric layer over said semiconductor substrate,

4 forming a gate over said gate dielectric layer,

5 forming gate sidewall spacers about said gate,

6 forming a source/drain having a heavily doped region recessed into said semiconductor  
7 substrate,

- 8 forming a salicide layer on said gate and said source/drain, and
- 9 forming metal contacts over said salicide layer on said gate and said source/drain.